REMARKS

Present Status of Application

Claims 1-21 remain pending in the application. The Office Action mailed October 05, 2004, rejected claims 1-21 under U.S.C. 102(b) as being anticipated by Tan et al. (US Patent No. 6,372,622).

Claims 1 and 16 have been amended. Applicant believes that these changes do not introduce new matter and reconsideration of those claims is respectfully requested. In view of the above amendments and the following discussions, a notice of allowance is respectfully solicited.

Discussion for 35 U.S.C. 102 rejections

Claims 1-21 were rejected under U.S.C. 102(b) as being anticipated by Tan et al. (US Patent No. 6,372,622).

Claims 1 and 16 have been amended to provide more detailed descriptions according to the present invention respectively. Supporting grounds for these amendments can be found in figures 3-10 and the related descriptions in page 5-7 of the specification. From figures 8-10 of this invention, it clearly shows that after reflowed, the solder bump 214a is formed on the second under-bump-metallurgy layer 210, without covering the sidewalls of the second under-bump-metallurgy layer 210.

As amended, independent claims 1 and 16 respectively recite:

Claim 1. A wafer bumping process, comprising the steps of:

providing a wafer, said wafer comprising a plurality of bonding pads and a passivation layer covering a surface of said wafer and exposing said bonding pads;

forming a first under bump metallurgy layer covering said passivation layer and said bonding pads;

forming a first patterned photoresist layer on said first under bump metallurgy layer, said first patterned photoresist layer comprising a plurality of first openings corresponding to said bonding pads and exposing a portion of said first under bump metallurgy layer;

forming a second under bump metallurgy layer within said first openings;

forming a second patterned photoresist layer on said first patterned photoresist layer, said second patterned photoresist layer comprising a plurality of second openings, said second openings being larger than said first openings to expose a portion of said second under bump metallurgy layer;

filling said second openings with a solder material, wherein the solder material covers said exposed portion of said second under bump metallurgy layer;

reflowing said solder material to form a plurality of solder bumps;

after reflowing said solder material, removing said second patterned photoresist layer and said first patterned photoresist layer to expose a portion of said first under bump metallurgy layer; and

removing said exposed portion of said first under bump metallurgy layer.

Claim 16. A structure of bumps comprising:

a substrate having at least an active surface;

a plurality of bonding pads formed on the active surface;

a passivation layer formed over the active surface of the substrate, wherein portions of the bonding pads are exposed by the passivation layer;

a first under bump metallurgy layer formed on the exposed portions of the bonding pads;

a second under bump metallurgy layer formed on the first under bump metallurgy layer; and

***a plurality of solder bumps formed on the second under bump metallurgy layer without covering sidewalls of the second under bump metallurgy layer,** wherein a melting point of the solder bumps is lower than a melting point of the second under bump metallurgy layer.*

Applicant respectfully asserts that the process of the amended claims 1 or the structure of claim 16 is patentably distinct from the prior art reference. Especially, the process comprises at least after reflowing said solder material, removing said second

patterned photoresist layer and said first patterned photoresist layer to expose a portion of said first under bump metallurgy layer, and the structure comprises at least a plurality of solder bumps formed on the second under bump metallurgy layer without covering sidewalls of the second under bump metallurgy layer.

Tan merely discloses a method for forming a bump structure including providing a device 10 having a bond pad 12, forming a barrier layer 14 and forming a first photoresist layer 20 with openings 22. Then, copper studs 30 are formed in openings 22 over the bond pads 12. Then, a second photoresist layer 40 is formed and solder bumps 60, 62 are plated on the copper studs 30. After removing the first and second photoresist layers 20, 40 and a portion of the exposed barrier layer 14, the plated solder bumps 60, 62 are reflowed. As clearly shown in Tan's Fig. 8, the reflowed bumps 60, 62 are substantially spherical and cover the sidewalls of the copper stud 30 and the remained barrier layer 14.

Obviously, Tan teaches reflowing the solder bumps after removing the photoresist layers and the barrier layer and after reflowed, the reflowed bumps covering the sidewalls of the copper stud 30 and the remained barrier layer 14.

Even considering that Tan's copper stud 30 was comparable to the second under bump metallurgy layer of this invention, according to the Office Action, Tan's teachings is different to and even against the features recited in the amended claims 1 and 16 of this invention.

On the contrary, according to the process steps of the present invention, the

reflow step is performed before removing the first and second patterned photoresist layers, so that the resultant bumps (after reflowing) will not overflow to cover the sidewalls of the underlying second under bump metallurgy layer. Hence, higher bumps are obtained, and the distance between the substrate and the wafer is increase, thus reducing the shear stress received by the bump and thereby increasing its mechanical reliability.

Accordingly, Tan fails to teach or disclose all limitations as recited in the amended independent claim 1 or 16. Claims 2-15 depend from claim1 and claims 17-21 depend from claim 16, and therefore are not anticipated by the reference Tan for the reasons noted above, as well as for the additional features recited therein. Therefore, reconsideration and withdrawal of these 102 rejections are respectfully requested.

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CONCLUSION

In view of the foregoing, it is believed that all pending claims are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,

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